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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,435	02/03/2004	Xudong Shi	RAMB-01015US1	3359

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VIERRA MAGEN MARCUS HARMON & DENIRO LLP
685 MARKET STREET, SUITE 540
SAN FRANCISCO, CA 94105

EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/770,435	SHI ET AL.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24 and 25* is/are allowed.

6)☒ Claim(s) *1-9,11-13,15-23,26-37* is/are rejected.

7)☒ Claim(s) *10 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's Amendment filed on 9-19-05 has been received and entered in the case. The rejections set forth in the previous Office Action are maintained as indicated below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 26-29, 31-32 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by the Fayneh et al reference (U.S. Patent 6,329,882).

Fayneh et al discloses in figure 2 an apparatus for carrying out a method of obtaining a current 222 from a charge pump 204 responsive to an input signal Fref, providing a bias current VBN to a circuit component in the circuit responsive to the current, and biasing the circuit component responsive to the bias current as required by claims 26 and 31.

As to claims 27-28, phase locked loop circuit and delay locked loop circuit are equivalent circuit as known in the art.

As to claim 29, Fayneh et al discloses the reference input signal being a clock reference signal (See Abstract).

As to claims 32 and 34, Fayneh et al discloses a phase mixer 202 and a clock buffer 228 as required by the claims.

3. Claims 1-9, 11-13, 15-23, 26-28 and 30-37 are rejected under 35 U.S.C. 102(e) as being anticipated by the Dietl et al (U.S. Patent 6,556,088).

Dietl et al discloses in figure 9 an apparatus comprising a voltage generator 95 for providing a current VBN representing frequency, an VCO 212 coupled to the voltage generator for providing a bias current V responsive to the current wherein the bias current being provided to a third circuit selected from the group consisting of a charge pump 91, a loop resistor 94,, a phase mixer 90, amplifier 93, clock buffer 97 and an equivalent 92 as required by claim 1-6. It is noted that there exists a current on an electrical conducting means due to resistivity of on a conducting means.

As to claim 7, Dietl et al discloses in figure 9 an apparatus comprising a phase-frequency detector 90 capable of providing a phase difference signal responsive to an input signal V0 and a feedback signal V, a first charge-pump 91, coupled to the phase-frequency detector, capable of providing a first voltage responsive to the phase difference signal, a second charge pump 92, coupled to the phase-frequency detector, capable of providing a second voltage responsive to the phase difference signal; a loop resistor 94, coupled to the first charge-pump, capable of providing a buffered voltage responsive to the first voltage, a voltage regulator 95, coupled to the loop resistor and the second charge pump, capable of providing a current responsive to the buffered voltage and the second voltage, wherein the voltage regulator includes a bias-generating device (see component 52 of figure 5) capable of providing a bias current VBN, a voltage-controlled oscillator 96, coupled to the voltage regulator, capable of providing the feedback signal responsive to the current, and an interconnect (i.e., connecting lines), coupled to the voltage

regulator, the first charge pump, and the second charge pump, capable of providing the bias current as required by claim 7.

As to claim 8, figure 5 (showing detail of voltage regulator 95) discloses the bias-generating device 52 comprising MOSFET device.

As to claim 9, figure 5 shows the MOSFET device being a p-type transistor having a drain coupled to the interconnect (by ways of other transistors) and a source coupled to a voltage source Vdd.

As to claims 11-13, the scopes of these claims are similar to that of claims 7-9. Therefore, they are rejected for the same reasons set forth above.

As to claim 15, figure 9 discloses a first circuit 94 capable of providing an output signal responsive to a comparison of an input signal V0 and a feedback signal V, and a second circuit 95, coupled to the first circuit, capable of providing a bias current VBN to the first circuit responsive to the input signal.

As to claims 16-18, figure 9 shows the first circuit including a first circuit component R being biased responsive to the bias current by way of charge pump 91.

As to claim 19, figure 5 (showing detail of voltage regulator 95) discloses the bias-generating device 52 comprising MOSFET device.

As to claim 20, figure 5 shows the MOSFET device being a p-type transistor having a drain coupled to the interconnect (by ways of other transistors) and a source coupled to a voltage source Vdd.

As to claim 21, figure 9 is commonly known as a phase locked loop circuit.

As to claim 22, phase locked loop circuit and delay locked loop circuit are equivalent circuit as known in the art.

As to claim 23, figure 9 discloses the first circuit including a voltage-controlled oscillator 96 having an input (i.e., terminal coupled to VBN), and the second circuit being capable of generating the bias current VBN proportional to input current provided to the voltage-controlled oscillator input.

As to claims 26-28 and 30-36, they are rejected for reciting method/step derived from the apparatus of claims 1-3, 7, 15-19 and 21-22.

As to claim 37, the scope of claim is similar to that claim 15. Therefore, it is rejected for the same reason set forth above.

Response to Arguments

4. Applicant's arguments filed 9-19-05 have been fully considered but they are not persuasive.

Regarding the rejection of claims under 35 USC 102 by the Fayneh reference, Applicant has argued that Fayneh discloses bias voltage VBN instead of current bias as required by claim 26. Examiner respectfully disagrees since voltage and current are electrically related via a fundamental equation V=RI. Voltage and current always co-exist on the same conducting means since voltage represents potential difference between two nodes and current represents density of charge flowing between two nodes. In fact, Applicant already knows about the above fact since Fig. 6 of the instant application shows terminal OUT including both voltage and current (i.e., Iid and Vreg).

As to claims 32 and 34, Applicant has argued that Fayneh does not disclose "a phase mixer" and "clock buffer" as recited in claims. Examiner respectfully disagrees since phase detector 202 of Fayneh is qualified to be considered phase mixer (i.e., mixing phase of the VCO 212); and feedback frequency divider 228 is a clock buffer since it buffers the clock signal provided at its input terminal. It also noted that bias voltage VBN of Fayneh provides to each and every component in his circuit (i.e., directly and/or indirectly).

Regarding the rejection of claims under 35 USC 102 by the Dietl et al reference, Applicant has argued that Dietl discloses bias voltage VBN instead of current bias as required by claim 1. Examiner respectfully disagrees for the same reason as noted above. As to *current representing frequency and/or delay,* Dietl does not explicitly disclose such terms. However, a current can be seen as a result derived from various factor, i.e., fluctuation of magnetic field, temperature, bias voltage, etc..., applied to a circuit. Therefore, a *current representing frequency and/or delay* limitation recited in claims 1 and 4 read on the reference. Further, the specification merely disclose "[C]urrent Iid represents frequency or delay information of the PLL or DLL" without further disclosing any particular element/component to provide such current. Thus, a current in Dietl is seen as a *current representing frequency and/or delay* since Dietl's circuit comprises components configured as required by claims. If the entire structure of the claimed invention is met by the teachings of the prior art, by necessity the functional limitations of the claims will also inherently be met. If the Applicant still believes that there is different functionality between their invention and that prior art, then Applicant's invention must have further elements and/or connections not met by the teachings of the prior art, where the additional elements/connections have not been recited in the claims.

As to claims 3 and 6, Applicant is reminded that the output voltage V is shown to provide, directly or indirectly, to each and every element within the apparatus.

As to claims 7-9 and 15, Applicant has argued VBN represents voltage which is not current as required by claims. Examiner respectfully disagrees for the reason set forth above.

As to claim 11, Applicant has argued that claim 11 calls for a delay locked loop circuit and a voltage-controlled delay line and Examiner had not identified these components in the cited prior art. Examiner respectfully disagrees since DLL and PLL circuits are seen as equivalent circuit as known in the art. A voltage controlled oscillator and a voltage controlled delay oscillator are identically configured apparatus (i.e., loop having phase detector, charge pump and oscillator). An oscillator is called a voltage controlled oscillator if changing frequency is an intended purpose; and is called a voltage controlled delay oscillator if matching phase is an intended purpose.

As to claim 36, see explanations pertaining claims 1 and 11.

As to claim 37, Examiner believes the scope of claim 15 and that of claim 37 are similar. The only difference between these claims is different terminologies, i.e., output signal vs. feedback; means vs. second circuit. It is noted that any component other than "a first circuit" and "a second circuit" is seen as a circuit component included in the first circuit.

Allowable Subject Matter

5. Claims 24-25 are allowed.

6. Claims 10 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to discloses an apparatus comprising elements being configured as recited in claims. Specifically, none of the prior art teaches or fairly suggests, among other things, a voltage regulator comprising nine transistors being configured specifically as recited in claims 10, 14 and 24.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
10-20-05 ATL

Kenneth B. Wells
Primary Examiner